A1 Concluded

4. (*Amended)* A backplane according to claim 1 wherein at least one of said two layers is modified in one of said spacer and said electrical or electronic element relative to the other of said spacer and said electrical or electronic element.

5. (*Amended)* A backplane according to claim 1 wherein all the layers in the spacer correspond in material and order to those found in the said at least one electrical or electronic element.

6. (*Amended)* A backplane according to claim 1 wherein the spacer is overall electrically insulating between top and bottom.

7. (*Amended)* A backplane according to claim 1 wherein there is a plurality of said spacers distributed over the backplane.

A2

9. (*Amended)* A backplane according to claim 7 wherein the array provides a plurality of addressable locations, and each location has at least one said spacer associated therewith.

A3

11. (*Amended)* A backplane according to claim 7 wherein at least one said spacer is in the form of a column having a generally square cross-section.

12. (*Amended)* A backplane according to claim 7 wherein at least one said spacer is in the form of a ridge having an elongate cross-section.

13. (*Amended)* A backplane according to claim 1 wherein said array is covered by an insulating layer which also extends over the said spacer or sad plurality of spacers.

A4

16. (*Amended)* A backplane according to claim 13 wherein an electrode is deposited on said insulating layer and is coupled to a said element of said array.

A5

19. (*Amended)* A backplane according to claim 1 wherein the top surface thereof is treated in a manner to induce liquid crystal alignment.

20. (*Amended)* A backplane according to claim 1 wherein the backplane is an active backplane in which the array comprises active electronic elements.

21. (*Amended)* A backplane according to claim 1 wherein at least some of the spacers are located externally of the array.

22. (*Amended)* A backplane according to claim 1 wherein the array is connected to other circuitry formed on the backplane but spaced from the array by a lane.

23. (*Amended)* A backplane according to claim 21 wherein said externally located spacers are located in said lane.

24. (*Amended)* A backplane according to claim 22 wherein the said lane is of sufficient width to permit the presence of an adhesive sealing strip without substantial contact with the array and said other circuitry.

25. (*Amended)* A backplane according to claim 22 wherein the width of the lane is at least 500 microns.

27. (*Amended)* A backplane according to claim 22 wherein the said circuitry connected to the array comprises logic for addressing elements of the array.

28. (*Amended)* A method of producing a backplane as defined in claim 1 wherein processes used for making parts of at least one said element are also used simultaneously to form parts of said spacers.

31. (*Amended)* A method of producing a backplane according to claim 29 wherein the spacers comprise at least two layers of substantially the same material and occurring in the same order as is found in at least one said electrical or electronic element.

32. (*Amended)* A cell comprising a backplane as defined in claim 1 and an opposed electrode sealed thereto in spaced relation.